

In the Claims:

1. (Currently Amended) A semiconductor chip comprising:
a semiconductor substrate comprising an active region;
a first structure formed on the active region, the first structure being fully silicided; and
at least one dummy silicide structure formed on the semiconductor substrate, wherein a shallow trench isolation extends under an entire width of a first dummy silicide structure of the at least one dummy silicide structure ~~is formed completely over an isolation region, the isolation region comprising a dielectric material in a recess in the semiconductor substrate.~~
2. (Original) The semiconductor chip of claim 1 wherein the first structure is a transistor gate electrode of a transistor.
3. (Original) The semiconductor chip of claim 2 wherein the transistor further comprises a gate dielectric underlying the first structure, the gate dielectric comprising a high permittivity dielectric selected from the group consisting of aluminum oxide, hafnium oxide, hafnium oxynitride, hafnium silicate, zirconium oxide, zirconium oxynitride, zirconium silicate, yttrium oxide, lanthalam oxide, cerium oxide, titanium oxide, and tantalum oxide.
- 4-5. (Cancelled)
6. (Previously Presented) The semiconductor chip of claim 1 wherein the first structure and the at least one dummy silicide structure each comprises nickel silicide.

7. (Previously Presented) The semiconductor chip of claim 1 wherein the first structure and the at least one dummy silicide structure each comprises a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.
8. (Previously Presented) The semiconductor chip of claim 1 wherein the first structure and the at least one dummy silicide structure each comprises germanium.
9. (Original) The semiconductor chip of claim 1 wherein the semiconductor substrate is a silicon substrate.
10. (Original) The semiconductor chip of claim 1 wherein the semiconductor substrate is a semiconductor-on-insulator substrate.
11. (Original) The semiconductor chip of claim 1 further comprising a contact etch-stop layer overlying portions of the first structure.
12. (Previously Presented) The semiconductor chip of claim 1 further comprising a dielectric layer overlying the first structure and the at least one dummy silicide structure.
13. (Currently Amended) An integrated circuit chip comprising:
 - a substrate having an active region and an isolation region;
 - a transistor formed on the active region, the transistor having a source region, a drain region, and a fully silicided gate electrode; and
 - at least one dummy silicide structure formed completely on the isolation region,

the at least one dummy silicide structure comprising a silicide layer and a dielectric layer, the dielectric layer being a separate layer from the isolation region and being interposed between the silicide layer and the isolation region.

14. (Previously Presented) The integrated circuit chip of claim 13 wherein electrical contacts are electrically coupled to the source region, the drain region, and the fully silicided gate electrode.

15-16. (Cancelled)

17. (Previously Presented) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and the at least one dummy silicide structure comprise nickel silicide.

18. (Previously Presented) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and the at least one dummy silicide structure comprise a silicide of a material selected from the group consisting of nickel, cobalt, copper, molybdenum, titanium, tantalum, tungsten, erbium, zirconium, and platinum.

19. (Previously Presented) The integrated circuit chip of claim 13 wherein the fully silicided gate electrode and the at least one dummy silicide structure comprise germanium.

20-43. (Cancelled)